IN THE CLAIMS:

Please cancel claims 22, 25, 29, 32, 23, 26, 30, 33 - 35, and 39 - 41. For convenience all claims are presented.

21. An inspection system comprising:

an inspection apparatus for detecting positions and sizes of particles or pattern defects on an object to be inspected;

an image taking apparatus for taking images of said particles or said pattern defects as detected by said inspection apparatus; and

an analysis unit operatively coupled to said inspection apparatus and said image taking apparatus, said analysis unit including:

a storage device for storing therein inspection data produced by said inspection apparatus and position information of regions of a circuit pattern to be formed on said object;

a calculation device for identifying particles and pattern defects that are correspondingly positioned in said regions, and calculating failure probabilities for said particles and said pattern defects positioned in said regions based on their sizes; and

a selection device for selecting particles or pattern defects whose calculated failure probabilities are greater than or equal to a predetermined threshold.

22 - 23. **These claims have been canceled in response to a restriction.**

24. The inspection system according to claim 21, wherein said regions are circuit blocks as formed within an LSI chip.

25 - 26. **These claims have been canceled in response to a restriction.**

27. The inspection system according to claim 21, further comprising a simulation device for generating virtual defects at random positions with respect to circuit graphics obtainable from mask layout data forming said circuit pattern, and computing

said failure probabilities from connection relationships of said circuit graphics and said defects.

28. The inspection system according to claim 21, wherein said position information of said regions is generated from mask layout data forming an LSI chip.

29 - 30. **These claims have been canceled in response to a restriction.**

31. The inspection system according to claim 24, wherein said position information of said circuit blocks is generated from mask layout data forming an LSI chip.

32 - 35. **These claims have been canceled in response to a restriction.**

36. A method for manufacturing semiconductor devices comprising the steps of:

a fabrication step for forming circuit patterns on or over a wafer, said circuit patterns constituting a plurality of semiconductor chips;

an inspection step for detecting positions and sizes of particles or pattern defects of said wafer;

identifying positions and sizes of those of said particles or said pattern defects located in a region of said circuit patterns that constitute one of said semiconductor chips;

a calculation step for calculating failure probabilities based on sizes of said pattern defects in said region;

an extraction step for extracting positions of said particles or said pattern defects with calculated failure probabilities greater than or equal to a predefined threshold; and

producing images of said particles or said pattern defects extracted at said extraction step.

37. A method for manufacturing semiconductor devices according to claim 36, wherein said regions are circuit blocks within an LSI chip.

38. A method for manufacturing semiconductor devices according to claim 37, wherein said LSI chip is a system LSI and said circuit blocks include memory portions and logic portions.

39 - 41. **These claims have been canceled in response to a restriction.**